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Enhancing the Design of VRM for Testing Magnetic Components

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ABSTRACT
The aim of this work is to design, build and test a voltage regulator module circuit (VRM) that can be used to compare the performance of different magnetic component designs. The VRM will be used to convert the input voltage (typically 12V) to a lower level which will supply a microprocessor load e.g. the Intel Pentium. The work will include review of VRM circuit topologies for VRM 10.1 specification. Circuit design will be performed for available controller IC. Simulation and analysis of the circuit in PSPICE and characterization under transient conditions, a circuit will be designed for simulating a transient load change in PSPICE.
Finally all required components will be ordered and the circuit will be built and can be used for testing of inductors and transformers.
Keywords: PSpice, Voltage regulator, Module, testing, magnetic components

I. INTRODUCTION

The increases in microprocessor speeds and transistor number have resulted in an increase in current demands and transition speeds. The supply voltages of the microprocessors have been decreased in order to reduce power consumption.

As Intel predicted, with the continuous advances being made with semiconductor technology, the microprocessors need to operate at significantly lower operating voltages, higher currents and higher slew rates.

These low voltages, high currents and high slew rates are the challenges imposed on power supplies for microprocessors.

The industry standard power supply architecture used is a dedicated DC-DC converter, the voltage regulator module (VRM), placed close to the microprocessor to minimize the impedance between the VRM and the microprocessor.

Voltage regulator modules are a special class of power converter circuits used to supply microprocessor loads e.g. the Intel Pentium. The VRM converts the system bus voltage (typically 12 V) to a lower level.

While current operating voltages are in the range of 1 - 1.5 V, it is expected that the required operating voltages in the next few years will decrease below 1 V while increasing the drawn current (the required current can easily exceed 100A) from the power supply in order to reduce the power consumption while increasing the microprocessor speed.

With such low voltage levels, one of the main challenges of VRM design is to maintain the constant output voltage under varying and transient load (current) conditions, when the microprocessor switches from one state to the other, voltage drop spikes occur, these spikes must be limited.

The main limit is caused by the large inductance values required to maintain ripple levels for steady-state operation. The standard industry solution is a multi-phase buck converter, in which the inductance is distributed between several phases that are controlled in parallel.

A buck derived voltage regulator module (VRM) will be designed to satisfy these requirements.

II. DESIGN PROCEDURE

This section summarizes a step-by-step procedure for a 12V-to-1.3V @120A power supply for high current and high transient speed applications.

- **Setting clock frequency**

R_T is an external resistor used to set the clock frequency. This clock frequency divided by the number of phases determines the switching frequency per phase. The switching frequency will be used to determine the size of the inductors and input and output capacitors and switching losses.

$$R_T = \frac{1}{n \times f_{SW} \times 4.5pF} - 27k\Omega$$

$$= \frac{1}{4 \times 485k\Omega \times 4.5pF} - 27k\Omega$$

$$= 87.55k\Omega$$

Where 4.5 pF and 27 kΩ are internal IC component values.

- **Soft Start & Current Limit Latch off delay times**

Soft start allows the power converter to gradually reach the initial steady state operating point, this reduces start up stress and surges. The

capacitor and resistor combination establish the soft start time.

$$C_{DLY} = \left\{20\mu A - \frac{V_{VID}}{2 \times R_{DLY}}\right\} \times \frac{t_{SS}}{V_{VID}}$$

Where t_{SS} is the desired soft start time of 2.5ms.

C_{DLY} = 40nF

Choosing the closest 1 % standard capacitor

C_{DLY} = 39nF

$$R_{DLY} = \frac{1.96 \times t_{DELAY}}{C_{DLY}}$$

= 452kΩ

Choosing the closest 5 % standard resistor

R_{DLY} = 470kΩ

- **Inductor Selection**

The choice of inductance for the inductor determines the ripple current in the inductor. The smaller the inductance the bigger the ripple current, which increases the output voltage ripple and conduction losses in the MOSFETs but the advantages are using smaller inductors and less total output capacitance.

$$L \geq \frac{V_{VID} \times R_O \times (1-(n \times D))}{f_{SW} \times V_{RIPPLE}}$$

$$\geq \frac{1.3V \times 1.3m\Omega \times (1-(4 \times 0.108))}{500kHz \times 18mV}$$

≥ 110nH

Choose inductor value

L = 105nH

$$I_R = \frac{V_{VID} \times (1-D)}{f_{SW} \times L}$$

= 22 A

I_R 50% of max DC current in inductor

Inductor should not saturate at peak current of 41 A

III. DCR (DC RESISTANCE)

The DCR is used for measuring the phase currents. A large DCR can cause excessive power losses, while too small a value can lead to increased measurement error.

DCR should be 1 - 1½ times droop resistance (R_O)

Use a DCR of 1.4mΩ

- **Output Droop Resistance**

The design requires that the regulator output voltage measured at the CPU pins drops when the output current increases. The specified voltage drop corresponds to a dc output resistance (Ro)

The output current is measured by summing the voltage across each inductor and passing the signal through a low-pass filter.

$$R_O = \frac{R_{CS}}{R_{PH(X)}} \times R_L$$

$$R_{PH(X)} = \frac{1.2m\Omega}{1.0m\Omega} \times 100k\Omega$$

= 120kΩ

- **Inductor DCR temperature correction**

The Inductor's DCR is used as the sense element and copper wire is source of the DCR, need to compensate for temperature changes of the inductors winding.

Temperature coefficient of copper = 0.39 % / ^{0}C = 0.0039

$$A = \frac{R_{TH(50^0C)}}{R_{TH(25^0C)}}$$

$$B = \frac{R_{TH(90^0C)}}{R_{TH(25^0C)}}$$

Relative values of RCS for each temperature 50^{0}C & 90^{0}C

$$r_1 = \frac{1}{1+(TC \times (T_1-25))}$$

= 0.9112

$$r_2 = \frac{1}{1+(TC \times (T_2-25))}$$

= 0.7978

Relative values for R_{CS1}, R_{CS2} and R_{TH}

$$r_{CS2} = \frac{(A-B) \times r_1 \times r_2 - A \times (1-B) \times r_2 + B \times (1-A) \times r_1}{A \times (1-B) \times r_1 - B \times (1-A) \times r_2 - (A-B)}$$

= 0.7195

$$r_{CS1} = \frac{(1-A)}{\frac{1}{1-r_{CS2}} - \frac{A}{r1-r_{CS2}}} = 0.3795$$

$$r_{TH} = \frac{1}{\frac{1}{1-r_{CS2}} - \frac{1}{r_{CS1}}} = 1.075$$

$R_{TH} = r_{TH} \times R_{CS}$ = 118.28kΩ

$$k = \frac{R_{TH(ACTUAL)}}{R_{TH(CALCULATED)}} = 0.8455$$

Calculate R_{CS1} and R_{CS2}

$R_{CS1} = R_{CS} \times k \times r_{CS1}$ R = 35.3kΩ

$R_{CS2} = R_{CS} \times ((1-k) + (k \times r_{CS2}))$ = 83.9kΩ

Choosing closest 1 % resistor gives:

R_{CS1} = 35.7 kΩ

R_{CS2} = 84.5kΩ

- **Output Offset**

The Intel specification requires that at no load the nominal output voltage of the regulator be offset to a value lower than the nominal voltage corresponding to the VID code.
Offset set by constant current source from FB pin through R_B

$$R_B = \frac{V_{VID} - V_{ONL}}{I_{FB}} = \frac{1.3V - 1.28V}{15.5\mu A}$$

= 1.29kΩ

Choosing closest 1 % standard resistor gives

R_B = 1.3 kΩ

- **C_{OUT} Selection**

Ceramic Capacitance
Use 18 X 10μF 1206 capacitors
Cz = 180 μF

Bulk Capacitance

$$Cx_{(MIN)} \geq \frac{L \times \Delta I_O}{n \times (R_O + \frac{\Delta V_{rl}}{\Delta I_O}) \times V_{VID}} - C_Z$$

$$\geq \frac{105nH \times 100A}{4 \times (1.25m\Omega + \frac{50mV}{100A}) \times 1.3V} - 180\mu F$$

= 1 mF

$$Cx_{(MAX)} \leq \frac{L}{nK^2 R_O^2} \times \frac{V_V}{V_{VID}} \times (\sqrt{1 + (t_V \frac{V_{VID}}{V_V} \times \frac{nKR_O}{L})^2} - 1) - C_Z$$

Where k = $-\ln(\frac{V_{ERR}}{V_V})$ = 5.2

* The VRM must be capable of accepting voltage level changes of 12.5 mV steps every 5 μs, up to 36 steps (450 mV) in 180 μs

V_V = 450 mV, t_V = 180 μs, V_{ERR} = 2.5 mV.

$$Cx_{(MAX)} \leq \frac{105nH \times 450mV}{4 \times 5.2^2 \times 1.25m\Omega^2 \times 1.3V} \times (\sqrt{1 + (\frac{180\mu s \times 1.3V \times 4 \times 5.2 \times 1.25m\Omega}{450mV \times 105nH})^2} - 1) - 180\mu F$$

$Cx_{(MAX)} \leq$ 27.3mF

Use eight 560 μF Al-Poly capacitors with a typical ESR of 5mΩ each yields Cx = 4.48 mF with an Rx = 0.63mΩ

$$Lx \leq C_Z \times R_O^2 \times Q^2$$

$$\leq$$

$$180\mu F \times 1.25m\Omega^2 \times 2 \leq$$ 563pF

Where Q is limited to $\sqrt{2}$ to ensure a critically damped system.

- **Power MOSFETS**

Guideline is to limit power dissipation to 1 W per MOSFET

Synchronous MOSFETs

With conduction losses being dominant
The power dissipated in each synchronous MOSFET

$$P_{SF} = (1-D) \times [(\frac{I_O}{n_{SF}})^2 + \frac{1}{12} \times (\frac{n \times I_R}{n_{SF}})^2] \times R_{DS(SF)}$$

$$= (1-0.108) \times [(\frac{120A}{8})^2 + \frac{1}{12} \times (\frac{4 \times 22A}{8})^2] \times 6.4m\Omega$$

P_{SF} = 1.34 W

Main MOSFETs

There are two main power dissipation components in main MOSFETs
Switching loss per main MOSFET:

$$P_{S(MF)} = 2 \times f_{SW} \times \frac{V_{CC} \times I_O}{n_{MF}} \times R_G \times \frac{n_{MF}}{n} \times C_{ISS}$$

$$= 2 \times 500kHz \times \frac{12V \times 120A}{8} \times 3\Omega \times \frac{8}{4} \times 800pF$$

= 864mW

Conduction loss per main MOSFET:

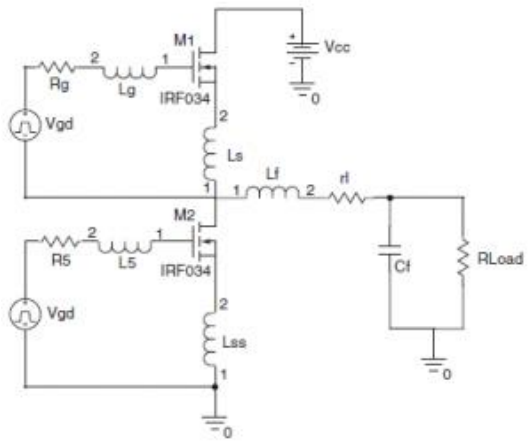
$$P_{C(MF)} = D \times [(\frac{I_O}{n_{MF}})^2 + \frac{1}{12} \times (\frac{n \times I_R}{n_{MF}})^2] \times R_{DS(MF)}$$

$$= 0.108 \times [(\frac{120A}{8})^2 + \frac{1}{12} \times (\frac{4 \times 22A}{8})^2] \times 23m\Omega$$

= 584mW

The power dissipated in each main MOSFET

P_{MF} = 1.45 W



Figure(1) The circuit Diagram

IV. CONCLUSIONS

The overall aim of this project was to design and build a voltage regulator module (VRM) so it could be used to test magnetic components. This goal was realized and switching circuit is ready for testing of inductors. A complete switching circuit is now fully completed and working. This can now be used for testing of different types and sizes of inductors and analyzing their performance.

The future for voltage regulator module (VRM) designers will be very demanding. As the currents increase and voltages decrease, stricter demands will be placed on the load line and thermal issues will become extremely important. In the future it is expected that the parasitic resistance between the regulator and microprocessor will become much more of an issue and it may be necessary to integrate the voltage regulator onto the microprocessor die but this will require a big breakthrough in silicon technologies.

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